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REMARKS

By the present amendment, claims 1, 12, and 23 have been amended. Claims 1-32 are pending in the present application. Reconsideration and allowance of outstanding claims 1-32 in view of the above amendments and following remarks are requested.

A. Rejection of Claims 1, 2, 4, 5, 10-13, 15, 16, and 21-23 under 35 USC §102(a)

The Examiner has rejected claims 1, 2, 4, 5, 10-13, 15, 16, and 21-23 under 35 USC §102(a) as being anticipated by U.S. Patent Number 6,182,203 B1 to Simar, Jr. et al. ("Simar"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 12, and 23, is patentably distinguishable over Simar.

The present invention relates to, in one embodiment, reducing power used when fetching instructions in a processor. One embodiment according to the present invention relates to very long instruction word ("VLIW") processors.

Execution of a computer program including, for example, VLIW packets residing in the computer's main memory, or external memory, involves fetching each VLIW packet from the computer's main memory into the processor. The fetching process takes a certain number of clock cycles and consumes a certain amount of power to transfer the instructions over the computer's internal data lines, or bus. Therefore, the more often instructions have to be fetched from main memory, the less time the processor has

available to decode and execute those instructions and the slower the speed at which the processor can finish tasks. Moreover, the more often instructions have to be fetched from main memory, the more power is used.

Referring to the present application, page 4, lines 6-17, the instruction cache approach has been inadequate for a number of applications. One of these applications is digital signal processing, where repetition of blocks of instructions (referred to as "instruction loops" or "repeat loops") is frequently encountered. Execution of a repeat loop involves refetching the instructions before they are repeated. The frequent refetching of repeated instructions consumes a significant amount of processor time and, in view of bus width considerations in VLIW processors, a relatively large amount of power. This drawback holds true even with the use of local memory techniques, such as with the use of an instruction cache.

Referring to the present application, in one embodiment the register queue comprises 16 registers, each storing a plurality of instructions (e.g. a VLIW packet). Advantageously, the register queue holds the 16 most recently executed VLIW packets, which can be quickly accessed consuming a relatively small amount of power. As disclosed in the present application, pages 26 and 27, an increment access signal, a repeat access signal, and a branch signal can be set. The signal that is set depends on which instruction is to be executed next. For example, at the end of an instruction loop the branch signal might be set in order to start the loop over from the beginning of the loop.

Applicants have amended independent claims 1, 12, and 23 in order to further

illustrate aspects of the present invention. For example, amended independent claim 1 recites, in part, "executing at least one instruction stored in a first register of said plurality of registers, setting an increment access signal to execute at least one instruction stored in a second register of said plurality of registers, wherein said second register is immediately in sequence after said first register."

Amended independent claims 12 and 23 recite similar limitations.

In contrast to the present invention as claimed, Simar is directed to a VLIW microprocessor comprising fetch circuitry, a first set of functional units, a second set of functional units, and dispatch circuitry. The dispatch circuitry is operable to dispatch each instruction of a given execution packet to both the first set of functional units and to the second set of functional units, such that all instructions of a given execution packet are executed in parallel. The dispatch circuitry selectively dispatches each instruction of each execution packet to either the first set of functional units or to the second set of functional units in response to a bit in each instruction.

The Examiner correctly states that Simar does not dislose the queue of the present invention. The Examiner asserts that Simar "must have" a storage, queue, or the like. However, in order to have a valid rejection under 35 USC §102(a), all of the elements must be disclosed within "the four corners" of the reference. Simar simply does not teach the novel queue arrangement of the present invention as defined by amended independent claims 1, 12, and 23 and as discussed herein. Therefore, Applicants respectfully request that the rejection under 35 USC §102(a) be withdrawn.

Moreover, Simar does not teach "executing at least one instruction stored in a first register of said plurality of registers, setting an increment access signal to execute at least one instruction stored in a second register of said plurality of registers, wherein said second register is immediately in sequence after said first register." Similarly, Simar does not teach the analogous language of amended independent claims 12 and 23.

Further, at column 14, lines 34, Simar explicitly states that "[i]nstructions are always fetched eight at a time." (Emphasis added). This recitation is a very narrow limitation that severely limits Simar's applicability to the present invention. This language means that Simar does not contemplate fetching more or fewer than eight instructions at a time. In fact, due in part to this language, Simar teaches against the present invention, which has no such inherent or explicit limitation. For example, amended independent claims 1 and 12 teach fetching a plurality of instructions. Amended independent claim 23 teaches fetching a plurality of VLIW packets.

Therefore, Simar does not disclose, teach, or suggest the present invention as defined by amended independent claims 1, 12, and 23, nor does Simar achieve some of the advantages of the present invention discussed herein. For example, Simar does not address the power consumption and speed issues as addressed by the claimed invention and discussed herein and in the present application.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claims 1, 12, and 23 is not taught, disclosed, or suggested by Simar. Thus, amended independent claims 1, 12, and 23 are

patentably distinguishable over Simar. As such, the claims depending from amended independent claims 1, 12, and 23 are, *a fortiori*, also patentably distinguishable over Simar for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. **Rejection of Claims 3, 6-9, 14, 17-20, and 24-32 under 35 USC §103(a)**

The Examiner has rejected claims 3, 6-9, 14, 17-20, and 24-32 under 35 USC §103(a) as being obvious with respect to Simar and U.S. Patent Number 5,926,832 to Wing, et al. ("Wing"). Applicants respectfully submit that claims 3, 6-9, 14, 17-20, and 24-32 depend from amended independent claims 1, 12, and 23, respectively, and thus, claims 3, 6-9, 14, 17-20, and 24-32 should be allowed at least for the same reasons discussed above in conjunction with patentability of amended independent claims 1, 12, and 23.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claims 1, 12, and 23 is not taught, disclosed, or suggested by Simar and Wing. Thus, amended independent claims 1, 12, and 23 are patentably distinguishable over Simar and Wing. As such, the claims depending from amended independent claims 1, 12, and 23 are, *a fortiori*, also patentably distinguishable over Simar and Wing for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. **Conclusion**

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 12, and 23, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-32 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-32 pending in the present application is respectfully requested.

Attorney Docket No.: 00CON104P

Respectfully Submitted,
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